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Design and Analysis of Ultra-Low Power Boost Converter using FinFET

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Abstract: The development of energy harvester circuits in recent decades have emerged a need of power efficient boost converter for the ultra-low power applications such as wireless sensor node etc. This paper proposed an optimized boost converter design using cross coupled finFET based LC resonant oscillator and FinFET charge pump circuit. The use of FinFET technology make this design robust for process, voltage and temperature (PVT) variation. This design generates 474.91 mV output voltage from 96 mV input voltage with power conversion efficiency of 42.90 %. It dissipates 30.03 nW power while feeding the 22.56 nW power to load.
Keywords: Boost Converter, Charge Pump, Energy Harvesting Circuits, FinFET, Ultra-Low Power Application

I. Introduction

The miniaturization of electronics system hasarisen the ultra-low power applications in different fields. These applications cover health sector monitoring smart devices, wireless sensor networks nodes and sensing devices in Internet of Things etc. [1]. These applications need mostly implantable smart devices having long life span. Therefore, these devices are powered with batteries. But, for having long life span, they increase the size of complete package or it required replacement of batteries again and again which is not feasible for all application. So, these applications require some alternative sustainable sources of power[2].
Recently, ambient power sources have engrossed the attention of research community towards the energy harvesting circuits. These ambient sources like thermoelectric generator, piezo-electric generators produce low voltage nearly less than 200 mV which is not sufficient for driving the application circuit. But still, these are good option for the replacement of batteries in ultra-low power application using an ultra-low power boost converter[3]. Therefore, main objective of this paper is to design ultra-low power boost converter while addressing the issues of start-up voltage, power conversion efficiency and power dissipation in the circuit etc. This paper is organized in sections as follow: overview of FinFET is given in section II. The next section III, covers the architecture of boost converter using FinFET technology. In section IV, simulating results of proposed design are discussed and finally section V conclude this work.

II. Overview of FinFET

The current-voltage characteristics of a NMOS device explain that the device operates in cut-off region for V_{GS} voltage lower than the threshold voltage V_{TH}. Ideally, it should have zero current but in reality, there exists a small drain current which is called as subthreshold current and this region is called as weak inversion region or subthreshold region [4]. In this region, diffusion of carrier take place which leads to exponential drain current with respect to V_{GS} voltage. This current is very significant in ultra-low power application.

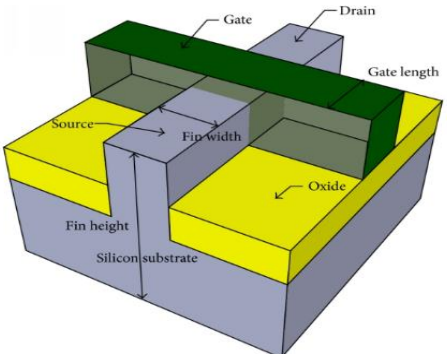

Fig.1: Basic structure of FinFET

The CMOS based conventional design of ultra-low power boost converters faces many process and performance related challenges. These challenges exist due to its operation in sub-threshold region where devices have more device-variation and low design margins [5]. Furthermore, the percentage of leakage power is also more in total power dissipation of a design working in sub-threshold region. This leakage

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power is caused due to the process variations as the technology advances. All these challenges make CMOS unfit for sub-threshold region operation in case of nano-scaled devices. This shifts the focus of researcher towards the other device option which has less short channel effects. Here, FinFET devices come in existence. FinFET devices are less sensitive to process, voltage and temperature (PVT) variation at sub-threshold region of operation in compare to CMOS device [6]. It has less leakage current. This robust nature of FinFET generates its application in ultra-low power regime.
Actually, FinFET have non planner channel which is covered with multi-gates from different directions. Therefore, it become as non-planner device and having channel in the shape of fin and called as FinFET (Fin Field Effect Transistor). Fig. 1 shows the basic structure of FinFET [7]. The manufacturing of this device is compatible with existing CMOS fabrication technology.

III. FinFET based Boost Converter Architecture

Boost converter design comprises of start-up circuit and multiplier circuitas shown in Fig. 2. Start-up circuit is used to initiate the operation from the very low input voltage harvested from ambient power source.

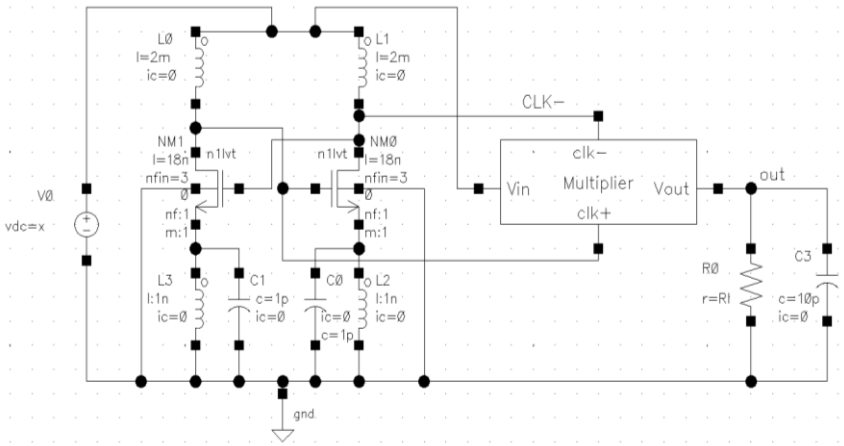

Fig. 2: Architecture of FinFET based boost converter

In this work, a LC resonant FinFET based cross coupled oscillator is used for starting the operation. This oscillator contains two n-FinFET devices which are cross coupled. Thus, out of these n-FinFET, only one conduct in subthreshold region due to low input voltage and at the same time other is completely in off state. Further, the cross coupled connection switches their state when a threshold voltage crosses. It makes first one in off state and second one in conduction state. So, this circuit is used for generating two phase sinusoidal clock signals viz. clk+ and clk-. These clocks are 180^0 out of phase from each other. The minimum input voltage of oscillator depends upon the value of L2, L3 and C0, C1 components. The frequency of oscillation is decided by the resonant load L1 inductor and capacitive load of multiplier circuit.

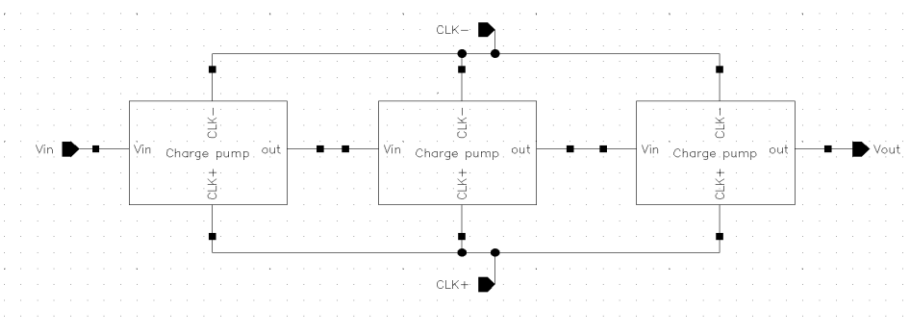

Fig. 3: Multiplier design having three number of charge pump stages

Here, normally used ring oscillator does not fit for low input voltage operation whereas LC resonant oscillator achieve the clock amplitude nearly two times the input voltage. But LC resonant oscillator use an inductor which increase the overall size of the design. So, it is a trade-off between performance and size of the design [8]. In the design of boost converter, a capacitor C3 and resistance R_L are connected at the load. This capacitor is used to suppress the ripples in the output dc voltage. As, its value increases, ripples decrease in the output but it also leads to more transition time for output voltage. So, its optimized value is required to

choose in the design. However, the load resistance should have same value as output resistance of boost converter to have impedance matching in the circuit. The maximum efficiency can be achieved only when there is no loading effect in the circuit.

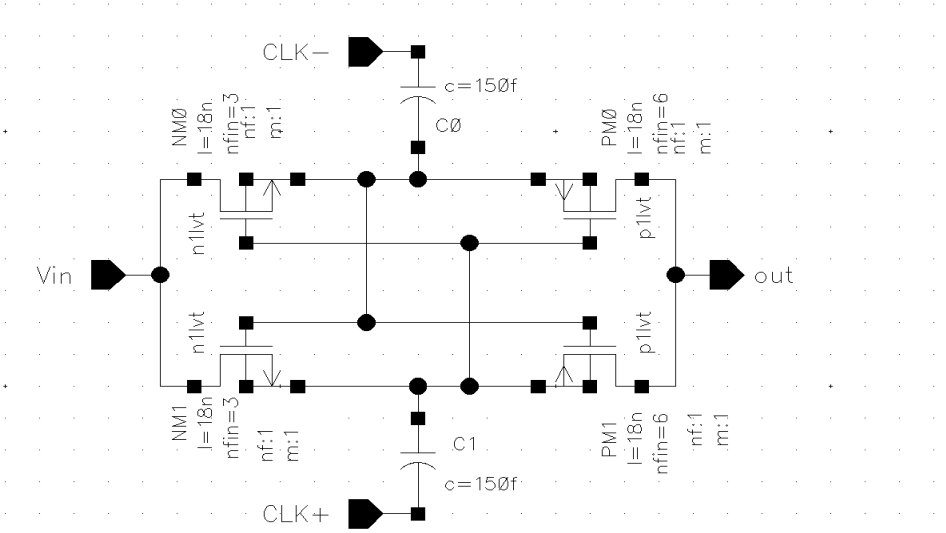

Fig. 4: FinFET based charge pump design

The clocks generated by oscillator are provided to next stage of multiplier circuit. Multiplier consists of n number of charge pump stages as shown in Fig. 3. Number of stages of charge pump depend upon the desired output voltage. A charge pump circuit have significant role in boost converter design. It is used for pumping the charge and in result boost the input voltage to a higher level. In this proposed architecture, n-FinFET NM0 and P-FinFET PM1 switches operates at the same time for charging and discharging of capacitor C0 and C1 respectively. In the other half cycle of clock, same task is performed by the NM1 and PM0 FinFETs. Thus, output voltage of charge pump become the sum of clock amplitude and discharged voltage across the capacitor[9].

Single stage of charge pump is sometime not sufficient to generate desired output voltage, so n number of stages of charge pump are used in its complete design. In this work, three number of charge pump stages are used. In design of charge pump as shown in Fig. 4, FinFET have replaced the CMOS technology. Here, FinFET suits better choice because initial charge pump stages are working in subthreshold region. Therefore, it reduces the leakage of power and conserve the harvested input voltage. P-FinFET are design here by taking six number of fins whereas n-FinFET have only three number of fins for having the equal current in the complete system. The output of charge pump works as input for the next stage whereas same clock signals are used for all the stages of charge pump. The capacitor C0 of each stage act as resonant load for the oscillator circuit. So, in case of three stages of multiplier, equivalent capacitance of parallel combination of these capacitor i.e. C0/3 decides the resonant frequency of the clock.

IV. Simulation Results

The simulation of proposed work is conducted on the Cadence tool using the 18nm FinFET technology. The FinFET library: Generic (cds-ff-mpt) 0.8V/1.8V FinFET/Multi Patterned 8 metal process design kit (PDK) is used for FinFET nodes. The values of component of boost converter is obtained by the optimization on the cadence tool for getting the desired results. The values of component L0 and L1 of the cross coupled resonant oscillator are selected to obtain optimized frequency for clock signal. Therefore, its size is large and decided to keep external to the chip. In proposed work, minimum input voltage is chosen as 96mV which is assumed to be generated by the harvested energy source and parallel impedance of 10 MΩ load resistance and 10 pF load capacitance is taken for the simulation of the results.

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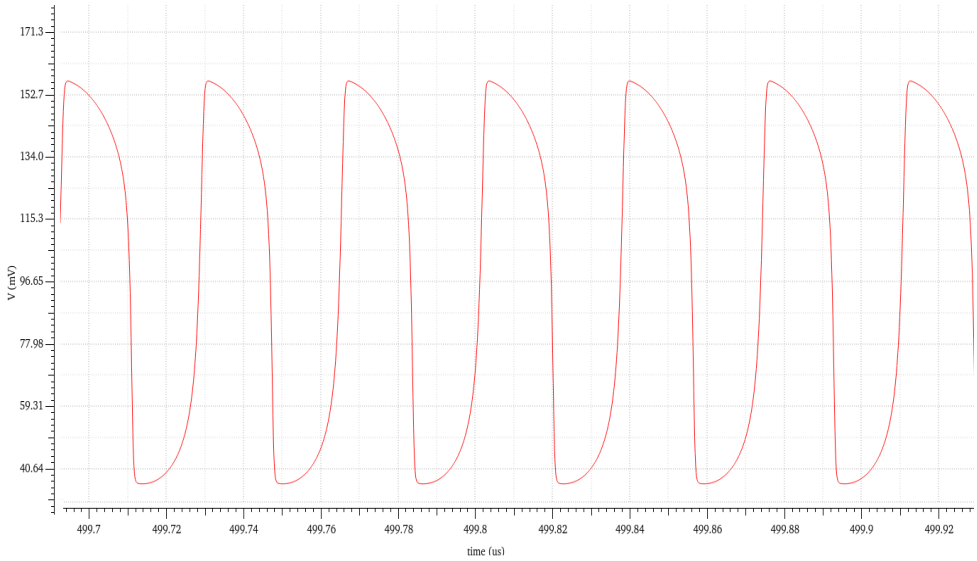

Fig. 5: Clock generated at 96mV input voltage

In Fig. 5, clock is represented which is generated by the LC resonant cross coupled oscillator. This clock has 157.73 mV amplitude and 19.96 MHz clock frequency when boost converter has come in its steady state. Its frequency and size of L0 or L1 inductor are related to each other. Decrease in inductor value can lead to have higher clock frequency, but it results in more dynamic power consumption in the system.
Fig. 6 illustrates the output voltage generated by the boost converter. In this work, 474.91 mV output dc voltage is achieved from the 96mV input voltage source. One of the advantages of this boost converter is its low transition time period. Here, output reaches in steady state nearly in 250 µs. The value of capacitor C0 in charge pump circuit is significant for these results. The higher output voltage is achieved in this work for smaller value of capacitor but it also increases the transient time period for the output. Its minimum value is limited by the parasitic value of capacitor in FinFET devices. As discuss earlier, ripples are controlled by the load capacitor C3. Thus, very small ripples having maximum amplitude of 0.12 mV are found in the output voltage of 474.91 mV which are less than 1% as compare to output voltage. So, a good quality DC output voltage is obtained in this work.

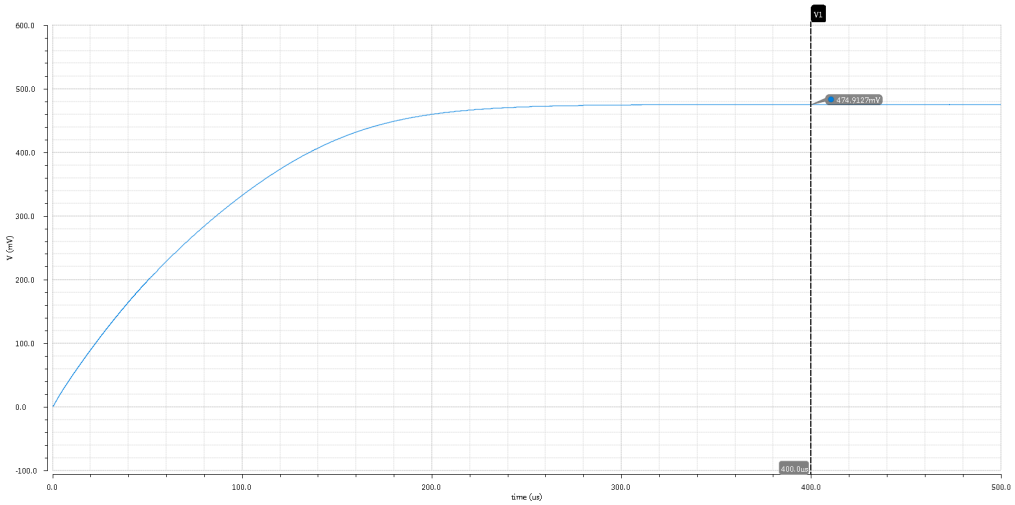

Fig. 6: Output voltage of boost converter at 96mV input voltage and 10MΩ load resistance

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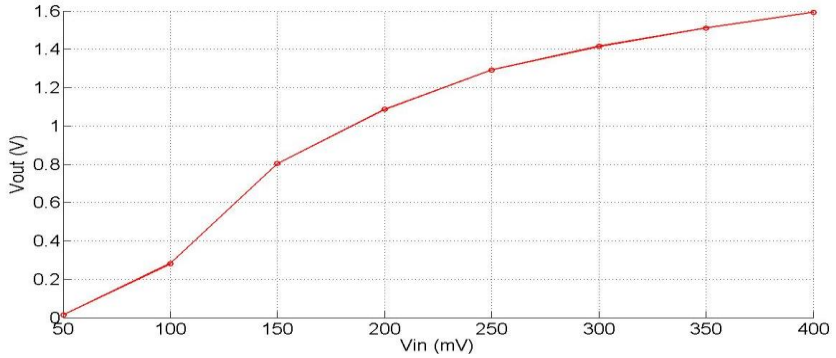

Fig. 7: Output voltage of boost converter at varying input voltage and 10MΩ load resistance

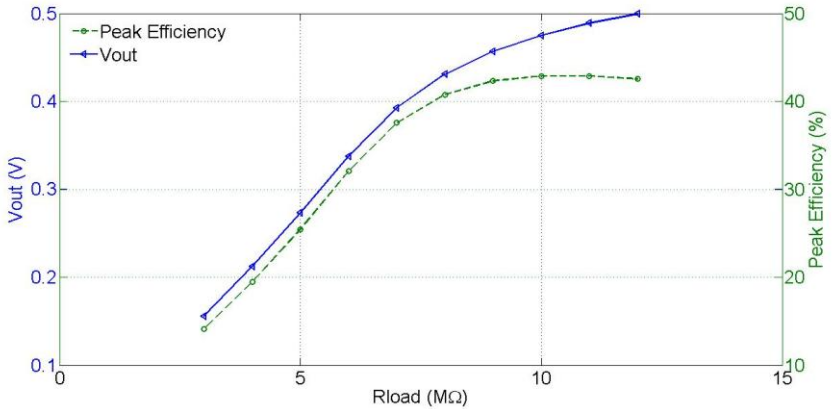

Fig. 8: Vout and peak efficiency vs load resistance at 96mV input voltage

Fig. 7 shows the output voltage for various input voltage at 10MΩ load resistance. As input voltage is increasing, output voltage also get increased. Therefore, better input harvester circuit will provide the more input voltage and in result, more output voltage. Fig. 8 shows the output voltage and peak efficiency results with variation in load resistance. Output voltage enhances as load resistance increased. In this work, maximum peak efficiency is achieved at 10MΩ load resistance. This is achieved due to perfect impedance matching at this load resistance. Before reaching this value, efficiency increases upto this mark and then decrease further. At 10MΩ load resistance, 52.59 nW power is extracted from the source and 22.56 nW power is fed to the load by the boost converter. Thus, boost converter achieved 42.90 % maximum peak efficiency and consume only 30.03 nW power.

Table 1: Comparison with other studies

Ref.	Process (nm)	Technology	Mini. Input Voltage (mV)	Output Voltage (mV)	Power Consumption (µW)	Peak Efficiency (%)
[8]	180	CMOS	96	420	0.23	24
[10]	65	CMOS	50	1200	16	73
[11]	130	CMOS	70	1250	12.31	58
This Work	18	FinFET	96	474.91	0.03	42.90

Table 1, makes a comparison with previously conducted studies. It can be depicted that proposed design consumes very less power as compare to other design and also achieve the good efficiency at the same time.

V. Conclusion

In this work, FinFET based optimized boost converter design is presented. It is constituted of LC resonant cross coupled oscillator and charge pump circuit. This design can be started at 96 mV input voltage. This boost converter provides the 474.91 mV output voltage with just consuming the 30.03 nW power. The ripples in the output voltage is found less than 1%. It has achieved the 42.90 % power conversion efficiency with 10 MΩ load resistance. This FinFET based design is found suitable for ultra-low power application with having pure dc output voltage and good efficiency which consumes very less power.

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